



FORM PTO - 1449				ATTORNEY DOCKET NO.: CDS-007			
INFORMATION DISCLOSURE STATEMENT				APPLICANTS: Bellantoni et al.			
				SERIAL NO.: 10/820,643			
				FILING DATE: 8-Apr-2004 GROUP: 2123			
U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
RG	A1	5,062,067	29-Oct-91	Schaefer et al.	364 703	578 16	15-Mar-89
RG	A2	5,437,037	25-Jul-95	Furuichi	395 717	700 146	7-Jun-93
RG	A3	5,502,661	26-Mar-96	Glunz	364 703	578 14	7-Oct-93
RG	A4	5,544,067	6-Aug-96	Rostoker et al.	364 703	488 14	14-Jun-93
RG	A5	5,696,942	9-Dec-97	Palnitkar et al.	395 703	600 17	24-Mar-95
RG	A6	5,768,567	16-Jun-98	Klein et al.	395 703	600 13	14-May-96
RG	A7	5,784,593	21-Jul-98	Tseng et al.	395 703	500 15	29-Sep-95
RG	A8	5,809,283	15-Sep-98	Vaidyanathan et al.	395 703	500 16	29-Sep-95
RG	A9	5,862,361	19-Jan-99	Jain	395 703	600 16	7-Sep-95
RG	A10	5,880,975	9-Mar-99	Mangelsdorf	364 703	378 15	5-Dec-96
RG	A11	5,978,571	2-Nov-99	Grundmann	395 703	500 23	12-May-97
RG	A12	5,991,523	23-Nov-99	Williams et al.	395 716	500 49	18-Mar-97
RG	A13	6,052,524	18-Apr-00	Pauna	395 703	500 43	14-May-98
RG	A14	6,134,516	17-Oct-00	Wang et al.	703	27	5-Feb-98
RG	A15	6,135,647	24-Oct-00	Balakrishnan et al.	395 716	500 18	23-Oct-97
RG	A16	6,152,612	28-Nov-00	Liao et al.	395 703	500 23	9-Jun-97
RG	A17	6,175,946 B1	16-Jan-01	Ly et al.	716	4	20-Oct-97
RG	A18	6,182,258 B1	30-Jan-01	Hollander	714	739	6-Feb-98
RG	A19	6,223,144 B1	24-Apr-01	Barnett et al.	703	22	24-Mar-98
RG	A20	6,295,517 B1	25-Sep-01	Roy et al.	703	15	7-Apr-98
RG	A21	6,321,363 B1	20-Nov-01	Huang et al.	716	4	11-Jan-99
RG	A22	6,466,898 B1	15-Oct-02	Chan	703	17	12-Jan-99
EXAMINER <i>R. Guld</i>				DATE CONSIDERED <i>5/27/2007</i>			

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FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
RG	C1	Andrews, J., Axis Systemss Inc., "Co-verification speeds SOC design," EDN, September 5, 2002, pp. 95-96, 98, 100.							
RG	C2	Axis Systems, Inc., "Xpert™ ARM® Solution," Datasheet, www.AxisSystems.com, 2 pages.							
RG	C3	Becker, M., "Faster Verilog Simulations Using a Cycle Based Programming Methodology," <i>Proceedings 1996 IEEE International Verilog HDL Conference</i> , Feb. 26-28, 1996, Santa Clara, CA, USA: IEEE Computer Society Press, 1996, pp. 24-31.							
RG	C4	Bell, G., "Solidification - Static Functional Verification with Solidify," HDAC, Inc., 8 pages.							
RG	C5	Björklund, D. et al., "A Language for Multiple Models of Computation," <i>Proceedings of the Tenth International Symposium on Hardware/Software Codesign</i> , May 6-8, 2002, Estes Park, CO, USA: CODES 2002, 2002 ACM, pp. 25-30.							
RG	C6	Braun, G. et al., "Using Static Scheduling Techniques for the Retargeting of High Speed, Compiled Simulators for Embedded Processors from an Abstract Machine Description," <i>International Symposium on System Synthesis</i> , Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 57-62.							
RG	C7	Chatelain, A. et al., "High-Level Architectural Co-Simulation Using Esterel and C," <i>Proceedings of the Ninth International Workshop on Hardware/Software Codesign/CASHE</i> , April 25-27, 2001, Copenhagen, Denmark: 2001 ACM, pp. 189-194.							
RG	C8	Choi, K. et al., "Incremental-in-time algorithm for digital simulation" <i>Proceedings of the Design Automation Conference</i> . Anaheim, June 12-15, 1988, <i>Proceedings of the Design Automation Conference</i> . Anaheim (DAC), New York, IEEE, US, vol. CONF. 25, 12-Jun-1988, pages 501-505.							
RG	C9	Clarke, P., "Cambridge startup claims speedier simulation tools," <i>EE Times</i> , http://www.eetimes.com/story/OEG2000424S0041 ; April 24, 2000, 2 pages.							
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OTHER ART, JOURNAL ARTICLES, ETC.		
RG	C10	Clarke, P., "EDA tool generates bit- and cycle-accurate C code," <i>EE Times</i> , http://www.eetimes.com/story/OEG20010713S0069 ; July 13, 2001, 1 page.
RG	C11	Clarke, P., "Tenison tool draws Verilog into SystemC compilation," <i>EEdesign</i> , http://www.eedesign.com/article/showArticle.jhtml?articleID=17406761 ; December 18, 2000, 2 pages.
RG	C12	Creusillet, B. et al., "Interprocedural analyses of Fortran programs" <i>Parallel Computing</i> , Elsevier Publishers, Amsterdam, NL, vol. 24, no. 3-4, May 1998, pages 629-648.
RG	C13	DeVane, C. J., "Efficient circuit partitioning to extend cycle simulation beyond synchronous circuits" <i>Computer-Aided Design</i> , 1997. Digest of Technical Papers., 1997 IEEE/ACM International Conference on San Jose, CA, USA 9-13 Nov. 1997.
RG	C14	Donnelly, K., "High performance VHDL simulation using native compiled code" <i>Electronic Engineering</i> , Morgan-Grampian LTD. London, GB, vol. 65, no. 803, 01-Nov.1993, page 51, 53, 55, 57.
RG	C15	Duarte, D. et al., "Evaluating the Impact of Architectural-Level Optimizations on Clock Power," <i>Proceedings of the 14th Annual IEEE International ASIC/SOC Conference</i> , Sept. 12-15, 2001, Arlington, VA, USA: 2001 IEEE, pp. 447-451.
RG	C16	Edwards, C., "Two startups jump into co-verification," <i>EEdesign</i> , http://www.design.com/article/printableArticle.jhtml?articleID=17407943 ; September 23, 2002, 3 pages.
RG	C17	Edwards, C., "U.K.'s Celoxica, Tenison enter co-verification fray," <i>Electronic Engineering Times</i> , October 14, 2002, pp. 24, 27.
RG	C18	Edwards, S. A., "Compiling Esterel into sequential code" <i>Proc Des Autom Conf; Proceedings - Design Automation Conference 2000 IEEE</i> , Piscataway, NJ, USA, 2000, pages 322-327.
	C19	French, R.S. et al., "A General Method for Compiling Event Driven Simulations," Stanford University, http://suif.stanford.edu/papers/rfrench95/paper.html; 19 pages.
RG	C20	Greaves, D., Tenison Technology, "VTOC Verilog -> C," <i>International Workshop on Rapid System Prototyping</i> , Tenison TechEDA, www.tenisontech.com , pp. 1-12.
RG	C21	Gupta, S. et al., "Conditional Speculation and its Effects on Performance and Area for High-Level Synthesis," <i>International Symposium on System Synthesis</i> , Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 171-176.
RG	C22	Hoffman, A. et al., "A Framework for Fast Hardware-Software Co-simulation," <i>Proceedings; Design, Automation and Test in Europe. Conference and Exhibition 2001</i> , Munich, Germany, March 13-16, 2001. IEEE Computer Society 2001, pp. 760-764.
RG	C23	International Search Report PCT/US 03/35649 dated 01-Dec-04
EXAMINER <i>R. G. G. G.</i>		DATE CONSIDERED <i>5/27/2007</i>

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OTHER ART, JOURNAL ARTICLES, ETC.		
RG	C24	International Search Report PCT/US 03/35403 dated 14-Dec-04
RG	C25	International Search Report PCT/US 03/35508 dated 05-Jan-05
RG	C26	Iyer, A. et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors," <i>Proceedings of the 29th International Symposium on Computer Architecture (ISCA '02)</i> , May 25-29, 2002, Anchorage, AK, USA: IEEE Computer Society 2002, pp. 158-168.
RG	C27	Joon-Seo, Yim, et al., "A C-based RTL Design Verification Methodology For Complex Microprocessor" <i>Proceedings of the Design Automation Conference</i> . Anaheim, June 9-13, 1997, New York, ACM, IS, vol. CONF. 34, 09-Jun-1997, pages 83-88.
RG	C28	Ju, Y-C, et al., "Incremental Circuit Simulation Using Waveform Relaxation" <i>Proceedings of the ACM/IEEE Design Automation Conference</i> . Anaheim, June 8-12, 1992, <i>Proceedings of the ACM/IEEE Design Automation Conference (DAC)</i> , Los Alamitos, IEEE Comp. Soc. Press, US, vol. CONF. 29, 08-Jun-1992, pages 8-11.
RG	C29	Jung, Y. et al., "simCore: an event driven simulation framework for performance evaluation of computer systems" <i>Modeling, analysis and simulation of computers and telecommunication systems</i> , 2000. <i>Proceedings. 8th International Symposium on San Francisco, CA, USA 29 Aug. - 1 Sept. 2002</i> .
RG	C30	Kim, M.G. et al., "Implementation of a Cycle-Based Simulator for the Design of a Processor Core," <i>Proceedings of AP-ASIC '99: The First IEEE Asia-Pacific Conference on ASICs</i> , Aug. 23-25, 1999, Seoul, South Korea: 1999 IEEE, pp. 108-111.
RG	C31	Kravitz, S.A. et al., "Massively parallel switch-level simulation : A feasibility study" <i>IEEE Inc. New York, US</i> , vol. 10, no. 7, 01-Jul-97, pages 871-894.
RG	C32	Krishnaswamy, V. et al., "Parallel Compiled Event Driven VHDL Simulation" <i>Conference Proceedings of the 1998 International Conference on Supercomputing ACM New York, NY, USA, July 1997</i> , pages 297-304.
RG	C33	Kudlugi, M. et al., "Static Scheduling of Multiple Asynchronous Domains for Functional Verification," <i>DAC 2001</i> , June 18-22, 2001, Las Vegas, Nevada, USA: 2001 ACM, 6 pages.
RG	C34	Liu, J. et al., "Software Timing Analysis Using HW/SW Cosimulation and Instruction Set Simulator," <i>Proceedings of the Sixth International Workshop on Hardware/Software Codesign (CODES/CASHE '98)</i> , March 15-18, 1998, Seattle, Washington, USA: 1998 IEEE, pp. 65-69.
RG	C35	Maurer, P.M, "Scheduling Blocks for Heirarchical Compiled Simulation," Technical Report DA-23, 1991, VCAPP Laboratory, University of South Florida, http://pangolin.csee.usf.edu/pub/facul.tv/maurer/tech-reports/da23_91.pdf , 23 pages.
RG	C36	McCammon, R. et al., "Cycle-accurate model speeds design," <i>EE Times</i> , http://www.eetimes.com/story/OEG19990615S0021 ; November 13, 2002, 6 pages.
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OTHER ART, JOURNAL ARTICLES, ETC.		
25	C37	Palnitkar, S. et al., Sun Microsystems, Inc., "Cycle Simulation Techniques," <i>Proceedings of the 1995 IEEE International Verilog HDL Conference</i> , March 27-29, 1995, Santa Cruz, CA, USA: IEEE Computer Society Press, 1995, pp. 2-8.
25	C38	Paul, J.M. et al., "Frequency Interleaving as a Codesign Scheduling Paradigm," <i>Proceedings of the Eighth International Workshop on Hardware/Software Codesign</i> , May 3-5, 2000, San Diego, CA, USA: CODES 2000, ACM 2000, pp. 131-135.
25	C39	Schulz, S.E., "Timing analysis tools in the critical path have a crucial impact on the success of a design," <i>EEDesign</i> , http:// www.eedesign.com/editorial/2000/focusreport0008.html ; November 13, 2002, 6 pages.
	C40	Stoye, W. et al., "Using Tenison VTOC™ for Large SoC Concurrent Engineering: A Real World Case Study," <i>GlobespanVirata</i>, TenisonEDA, www.tenison.com; pp. 1-13.
25	C41	Sun Young Hwang, "Incremental algorithms for digital simulation" <i>Integration, The VLSI Journal</i> , North-Holland Publishing Company. Amsterdam, NL, vol. 7, no. 1, 01-Apr-1989, pages 21-34.
25	C42	Tabbara, B. et al., "Fast Hardware-Software Co-Simulation Using VHDL Models," <i>Proceedings; Design, Automation and Test in Europe. Conference and Exhibition</i> , 1999, Munich, Germany, March 9-12, 1999. IEEE Computer Society 1999, pp. 309-316.
	C43	TenisonEDA, "Engineering Management in the SOC Era," www.tenison.com, 1 page.
	C44	TenisonEDA, "Hardware/Software Co-Design in the SOC Era," www.tenison.com; pp. 1-7
25	C45	TenisonEDA, "Introducing VTOC™: Bridging the SOC Co-Development Gap," <i>Tenison EDA World Tour</i> , September 2002, www.tenison.com , 14 pages.
	C46	TenisonEDA, "VTOC 1.0 User Guide," www.tenison.com; pp. 1-51.
	C47	Tenison Technology, "A Verilog to C Compiler," <i>Submitted to IEEE Transactions on Software Engineering</i>, pp. 1-10
25	C48	Tenison Technology: Hardware & Software Working Together, "New cycle-based Verilog Compiler is 50 to 100 times faster than behavioural simulation," www.tenisontech.com/news/nw010302.htm ; March 1, 2002, 1 page.
25	C49	Tensilica, "Synopsys and Tensilica Partner to Provide New Cycle-Accurate Model Generation Platform," http://www.tensilica.com/html/pr_2000_05_24.html ; November 13, 2002, 3 pages.
25	C50	Ye, W. et al., "The Design and Use of SimplePower: A Cycle-Accurate Energy Estimation Tool," <i>Proceedings of the 37th Design Automation Conference</i> , Los Angeles, CA, USA: DAC 2000, 2000 ACM, pp. 340-345.
EXAMINER <i>R. G. G. 10</i>		DATE CONSIDERED <i>5/27/2007</i>